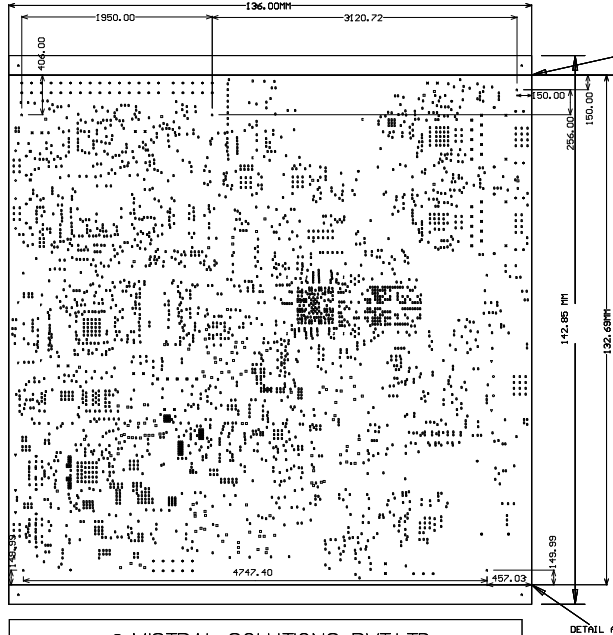


Symbol	Count	Hole Size	Plated	Routed Path Length	Hole Length	Hole Type
□	3154	6.00mil (0.203mm)	PTH	-	-	Round
□	119	10.00mil (0.254mm)	PTH	-	-	Round
□	4	22.00mil (0.559mm)	PTH	26.00mil (0.660mm)	48.00mil (1.219mm)	Slot
★	4	24.00mil (0.610mm)	PTH	38.00mil (0.965mm)	62.00mil (1.575mm)	Slot
▼	4	24.00mil (0.610mm)	PTH	38.00mil (0.965mm)	62.00mil (1.575mm)	Slot
F	4	26.00mil (0.660mm)	PTH	20.00mil (0.508mm)	46.00mil (1.168mm)	Slot
▽	2	28.00mil (0.711mm)	PTH	90.00mil (2.286mm)	118.00mil (2.997mm)	Slot
⊙	4	32.00mil (0.813mm)	NPTH	-	-	Round
J	2	34.00mil (0.864mm)	NPTH	-	-	Round
■	4	34.00mil (0.864mm)	PTH	34.00mil (0.864mm)	68.00mil (1.727mm)	Slot
⊗	20	36.00mil (0.914mm)	PTH	-	-	Round
⊗	5	40.00mil (1.016mm)	PTH	-	-	Round
⊗	66	40.00mil (1.016mm)	PTH	-	-	Round
E	1	44.00mil (1.118mm)	PTH	-	-	Round
⊗	14	44.00mil (1.118mm)	NPTH	-	-	Round
○	2	48.00mil (1.219mm)	NPTH	-	-	Round
D	1	62.00mil (1.575mm)	NPTH	-	-	Round
⊙	2	66.00mil (1.676mm)	NPTH	-	-	Round
○	4	66.00mil (1.676mm)	PTH	-	-	Round
I	4	68.00mil (1.727mm)	NPTH	-	-	Round
A	11	108.00mil (2.743mm)	NPTH	-	-	Round
C	1	118.00mil (2.997mm)	PTH	-	-	Round
XI	4	126.00mil (3.200mm)	NPTH	-	-	Round
3430 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DRILL TOLERANCE:

FOR 8 mil drill: ± 0.008 mil
FOR 10mil drill: ± 0.010 mil
FOR PTH ± 0.003 mil
FOR NPTH ± 0.002 mil
FOR 40 mil drill: ± 0.002 mil



DETAIL-A (V-GROOVE DETAILS)
SCALE: NTS

IMPEDANCE SPECIFICATIONS


SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01	EDGE COUPLED MICROSTRIP	L1L6	4	4.5	90	L2L5
02	EDGE COUPLED MICROSTRIP	L1L6	3.5	5.8	100	L2L5
03	EDGE COUPLED STRIPLINE	L3	4	4.5	90	L2L4
04	EDGE COUPLED STRIPLINE	L3	3.2	10	100	L2L4
05	MICROSTRIP	L1L6	5.2	-	50	L2L5
06	STRIPLINE	L3	3.7	-	50	L2L4

LAYER STACKUP

LAYER NAME	FINISHED Cu	X-SECTION	DIELECTRIC THICKNESS [INCHES]
SILKSCREEN TOP			
SOLDERMASK TOP			
L01 TOP	1oz.		0.0041
L02 L2-GROUND-1	1oz.		0.0039
L03 L3-SIGNAL-1	1oz.		0.020
L04 L4-POWER	1oz.		0.0039
L05 L5-GROUND-2	1oz.		0.0041
L06 BOTTOM	1oz.		
SOLDERMASK BOTTOM			
SILKSCREEN BOTTOM			

FAB NOTES :

- FABRICATE PCB IN ACCORDANCE WITH IPC-6012D, CLASS 2; PER IPC-6011.
- MATERIALS:
 - LAMINATE AND PREPREG (B-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126. (MIN.TG 170)
 - COPPER FOIL TO BE IN ACCORDANCE WITH IPC-HF-150. UNLESS OTHERWISE SPECIFIED, ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS AND INNER PLANE LAYERS TO BE 35UM (1 OZ.). FOR OUTER LAYERS 35UM (1 OZ.), COPPER WEIGHT IS TO BE CONSIDERED FINISHED. THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 6012B TABLE NO.3-7 AND 3-8.
- ALL HOLES SHALL BE LOCATED WITHIN 0.15MM DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
- BOW AND TWIST SHALL NOT EXCEED MORE THAN 0.75% OF THE DESIGN LENGTH.
- CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCREASE FOR MATCHING IMPEDANCE MISTRAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING. TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
- BOARD FINISHED SHALL BE ACCORDING TO IPC-6012D CLASS 2.
- AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
- FINISH:
 - ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG, ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
 - APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SH-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER. VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK. ONLY SOLDER MASK IMAGES THAT ARE 0.08(0.003) PER SIDE SHALL BE REDUCED IF REQUIRED. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
 - SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
 - SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM (0.00079), IN CASE OF LASER VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM (0.00047) AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM (0.0006).
 - ALL HOLES SURROUNDED BY LAND <=0.010 SHALL BE COMPLIANCE TO IPC6012, CLASS 2.
- MARKING:
 - BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO, MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
- TEST REQUIREMENTS:
 - 100% NET LIST ELECTRICAL VERIFICATION USING MISTRAL SUPPLIED IPC-D-356 NET LIST FOR OPENS AND SHORTS.
- THEIVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
- TEAR DROPS SHALL BE ADDED ON VIA'S AND THROUGH HOLE PADS IN ALL INTERNAL AND OUTER LAYERS.
- ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IF REQUIRED.
- FINISHED PCB THICKNESS SHALL BE 0.0620 ± 0.0010 .
- MIN TRACE WIDTH-SPACING ON BOARD IS 0.0032 / 0.0032.
- BOARD DIMENSIONS ARE IN MM

 MISTRAL SOLUTIONS PVT.LTD., #60, ADARSH REGENT, 100'FT RING ROAD, DOMLUR EXTENSION, BANGALORE-560 071			
TITLE:	PROC181E1-1 AM62L_EVM	REV	E1-1
DATE:09JULY25	6/6/2025	SCALE: 1	SHEET 16 OF 16

SIZE	DRAWING NO.	REV
C	PROC181E1-1	E1-1
SCALE:NONE		